SQ333

数据手册

N1-Channel + N2-Channel+ P-Channel

Three-in-one Enhancement Mode Field Effect Transistor

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Description

The SQ333 is Three-in-one enhancement mode MOSFET in a plastic package using the Trench technology. These features combine to make this design an extremely efficient and reliable device for variety of DC- DC applications.

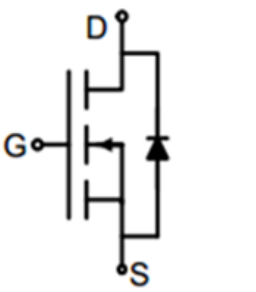
General Features

- Trench Technology
- Fast Switching
- Logic Level Compatible
- SMD Package (SOP8)

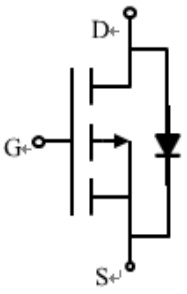
Application

- High Speed Switch
- DC-DC Converters
- Lithium-Ion Battery

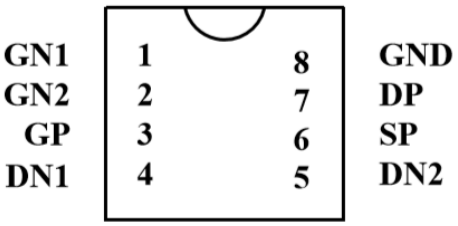
MOSFET Type	VDS(V)	VGS(V)	Vth Max(v)	RDS(ON)(mΩ)	ID(A)
NMOS1	23	±14.5	0.6	660	0.5
NMOS2	23	±14.5	0.6	660	0.5
PMOS	-12	±3.5	-0.57	500	-0.6



NMOS Schematic diagram



PMOS Schematic diagram



脚位	名称	极性	说明
1	GN1	G	NMOS1 的栅极
2	GN2	G	NMOS2 的栅极
3	GP	G	PMOS 的栅极
4	DN1	D	NMOS1 的漏极
5	DN2	D	NMOS2 的漏极
6	SP	S	PMOS 的源极
7	DP	D	PMOS 的漏极
8	GND	S	NMOS1 和 NMOS2 的源极

NMOS1 Absolute Maximum Ratings (T_A = 25 ℃, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	23	V
Gate-Source Voltage	V_{GS}	±14.5	V
Continuous Drain Current (Tc =25 ℃)	I_D	0.5	A

NMOS2 Absolute Maximum Ratings (T_A = 25 ℃, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	23	V
Gate-Source Voltage	V_{GS}	±14.5	V
Continuous Drain Current (Tc =25 ℃)	I_D	0.5	A

PMOS Absolute Maximum Ratings (T_A = 25 ℃, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	±3.5	V
Continuous Drain Current (Tc =25 ℃)	I_D	-0.6	A

Electrical Characteristics (T_A = 25 ℃, unless otherwise noted)

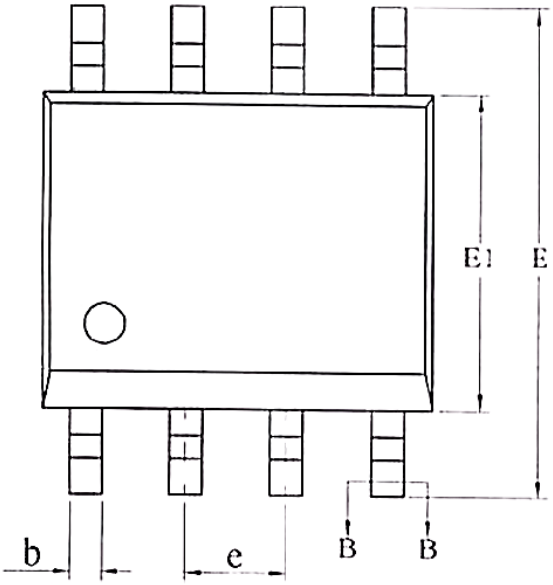
Parameter	Symbol	Condition	Min	Typ	Max	Unit
NMOS1						
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 10μA		23		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA		0.6		V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 100mA		660		mΩ
		V_{GS} =4.5V, I_D = 200mA		665		mΩ
NMOS2						
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 10μA		23		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA		0.6		V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 100mA		660		mΩ
		V_{GS} =4.5V, I_D = 200mA		665		mΩ
PMOS						
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA		-12		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA		-0.57		V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 0V, I_D = -100mA		-500		mΩ
		V_{GS} =0V, I_D = -200mA		-515		mΩ

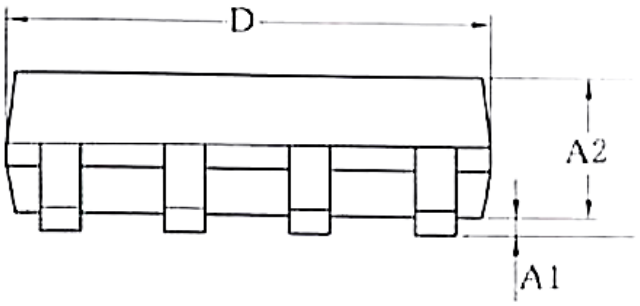
Note:

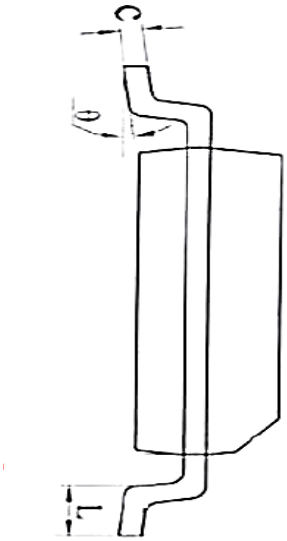
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

SOP8 Package Information

Dimensions in Millimeters (UNIT:mm)







SYMBOL	MIN	NOM	MAX
A1	0.03	-	0.10
A2	1.20	1.40	1.60
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
b	0.38	-	0.51
e	1.27BSC		
L	0.50	0.60	0.70
c	0.25BSC		
θ	0	-	10°

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.

Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

修改记录

版本	日期	描述
Ver1.00	2020-08-25	第一版

芯圣电子

2020 年 10 月